

# A Network Time Server Based on FPGA Hardware

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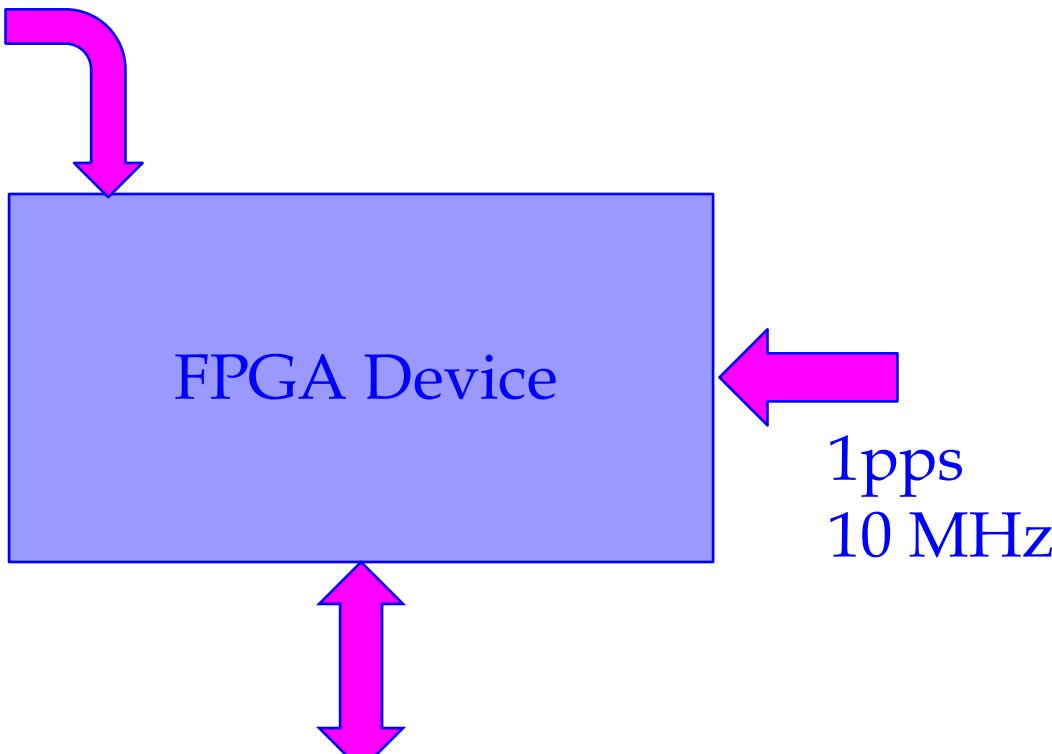
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# Motivation

- Single FPGA device supports full NTP load on 1Gb network circuit
  - Network maximum  $\sim 10^6$  NTP requests per second
- FPGA hardware simpler and much cheaper than the multiple servers that are now used
  - Single server supports  $2 \times 10^5$  requests/s
  - Multiple servers degrade delay stability when total load approaches circuit capacity (see backup slides)
- FPGA hardware much more secure
  - No OS vulnerabilities, or unsupported operating system
  - No network maintenance or control messages
    - *These require computer cycles to ignore the request*
  - No denial-of-service attacks on non-NTP ports
    - *Open ports required for control and maintenance*
    - *a serious problem with the current servers*

# High-Level Configuration

USB Port  
Command  
and  
control



1Gb Network connection, UDP/123  
NTP *time* requests only

# USB Commands

- Return number of NTP requests
- Initialize NTP seconds register
- Read NTP seconds register
- Set two leap second bits
  - 0=ok, 1=ls+, 2=ls-, 3=unsynchronized
- Set IP address of FPGA
- Set address of gateway
- Enable (=1) or disable(=0) network

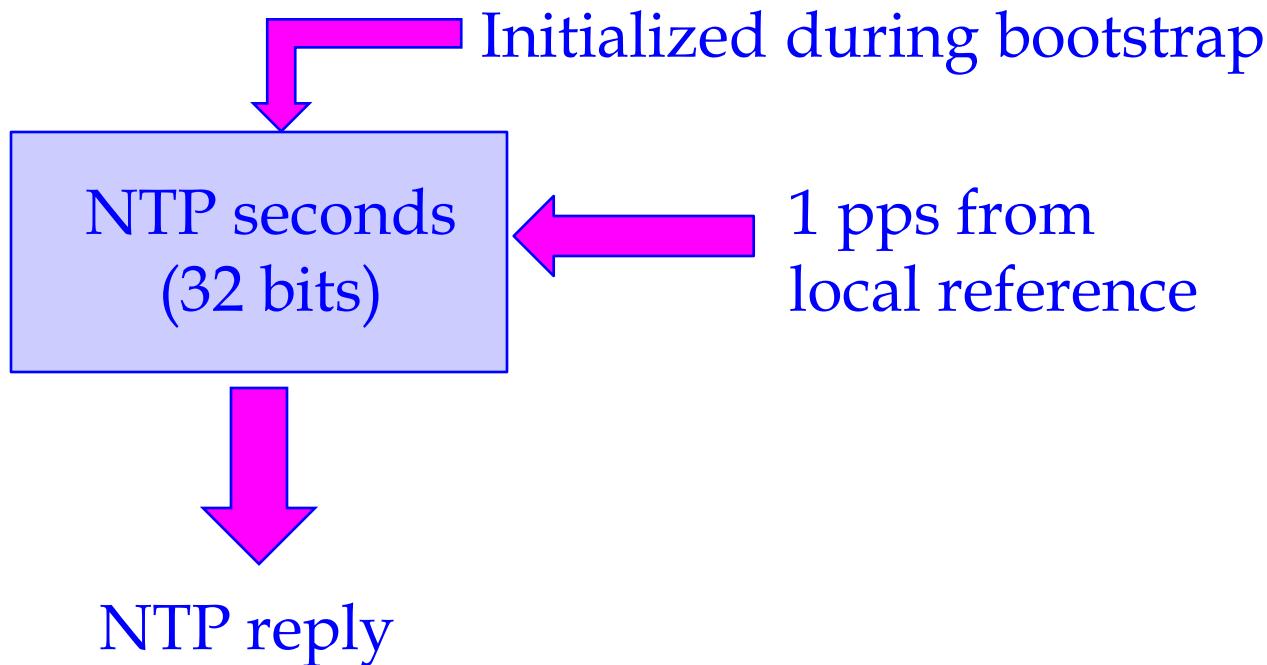
# Network Interface

- Packet Badger
  - Lawrence/Berkeley National Laboratory
  - <https://github.com/BerkeleyLab/Bedrock>
- Supports UDP messages at full network speed of 1 GB/s
  - NTP message ~ 1000 bits including network overhead in message
- Listens on UDP port 123 only
- Accepts NTP requests from any client IP address and port

# NTP Time Format

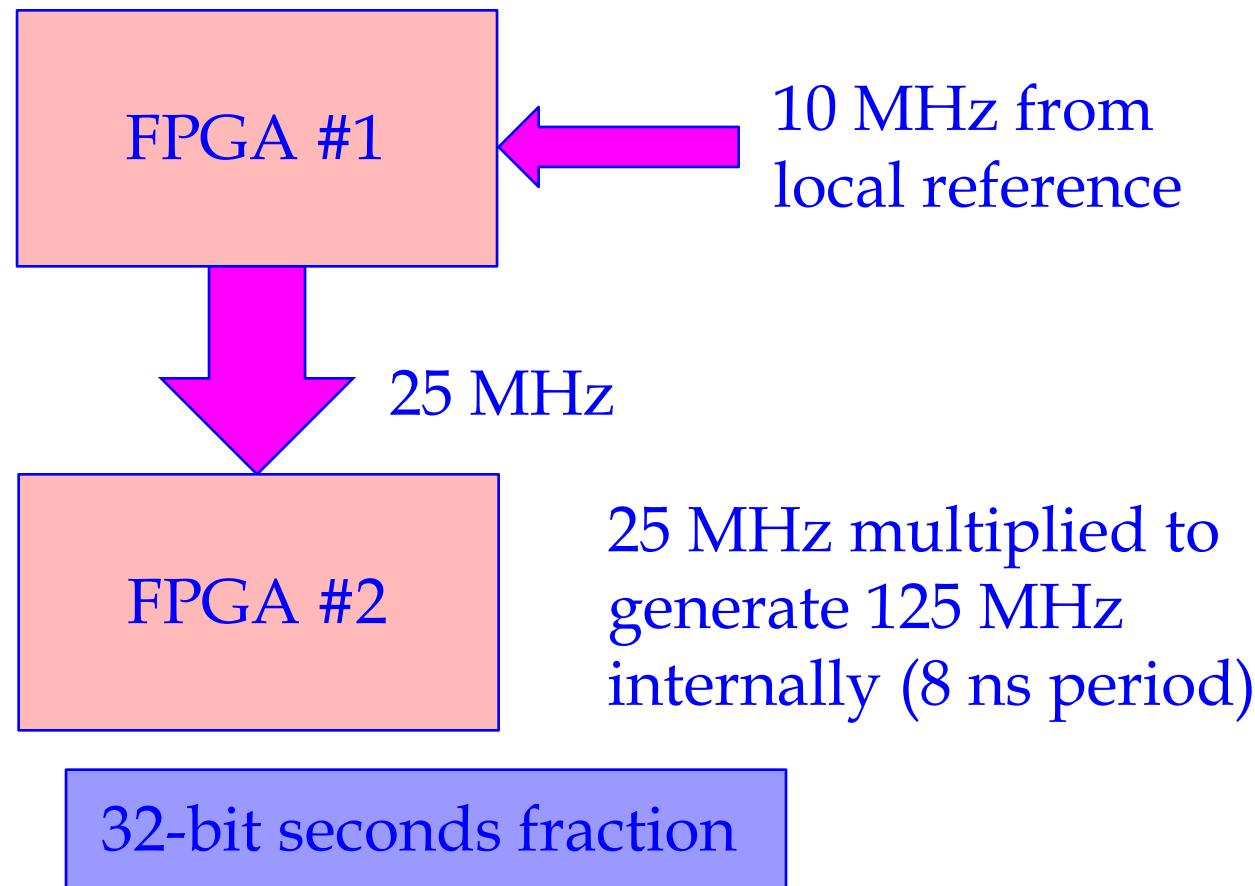
- 64-bit integer
  - 32-bit unsigned integer seconds since 1900.0
    - Least significant bit= 1 second
    - Maximum value=  $(2^{32} - 1)$  s  $\sim$  136+ years
  - 32-bit unsigned integer seconds fraction
    - Least significant bit =  $2^{-32}$  s  $\sim$  232.83064 ps
    - Maximum value= 1s - 232.8 ps
- NTP time value must be generated from external 1 pps and 10 MHz with no multiplications or divisions

# Generating NTP seconds - 1



NTP seconds, unsigned 32-bit integer  
origin is 1900.0. Incremented on external pulse

# Generating NTP fraction - 1



8 ns “tick” =  $2^{32}/125 \times 10^6 = 34.35973$  counts in fraction

# Generating NTP fraction - 2

- $R$ = register holding NTP fraction
- $C_1, C_2, C_3, C_4$  internal registers
  - Add 1 to all C registers on every 8 ns tick
- Increment register  $R$  by 34 every 8 ns tick
- When  $C_1=100$ : add 35 to  $R$ , set  $C_1=0$
- When  $C_2= 1000$ : add 9 to  $R$ , set  $C_2=0$
- When  $C_3 = 10000$ : add 7 to  $R$ , set  $C_3= 0$
- When  $C_4= 100 000$ : add 3 to  $R$ , set  $C_4= 0$
- Reset all counters on 1 pps pulse
- Time error  $< 1 \mu\text{s}$  for all values

# Results of tests

- Time to process a request
  - FPGA: 330 ns
  - Operating server: 4.4  $\mu$ s (13  $\times$  FPGA)
- NTP message accuracy on local network about 5  $\mu$ s for both systems – limited by network jitter
- FPGA system has better stability, but stability limited by network jitter even on local network
- Network jitter  $\sim$  white phase + flicker phase
  - Some improvement with averaging
    - Statistical distribution not stationary

# Summary

- FPGA NTP server synchronized to 1 pps and 10 MHz signals from local clocks
- NTP server based on FPGA hardware cheaper and faster than servers based on commercial systems
- First server now publicly available on University of Colorado network (IP=128.138.140.211)
- *FPGA system has better network security, less sensitive to attacks*
  - *Maintenance and control through separate USB-based connection*

Extra slides if time available

# FPGA server on 1 Gb/s network

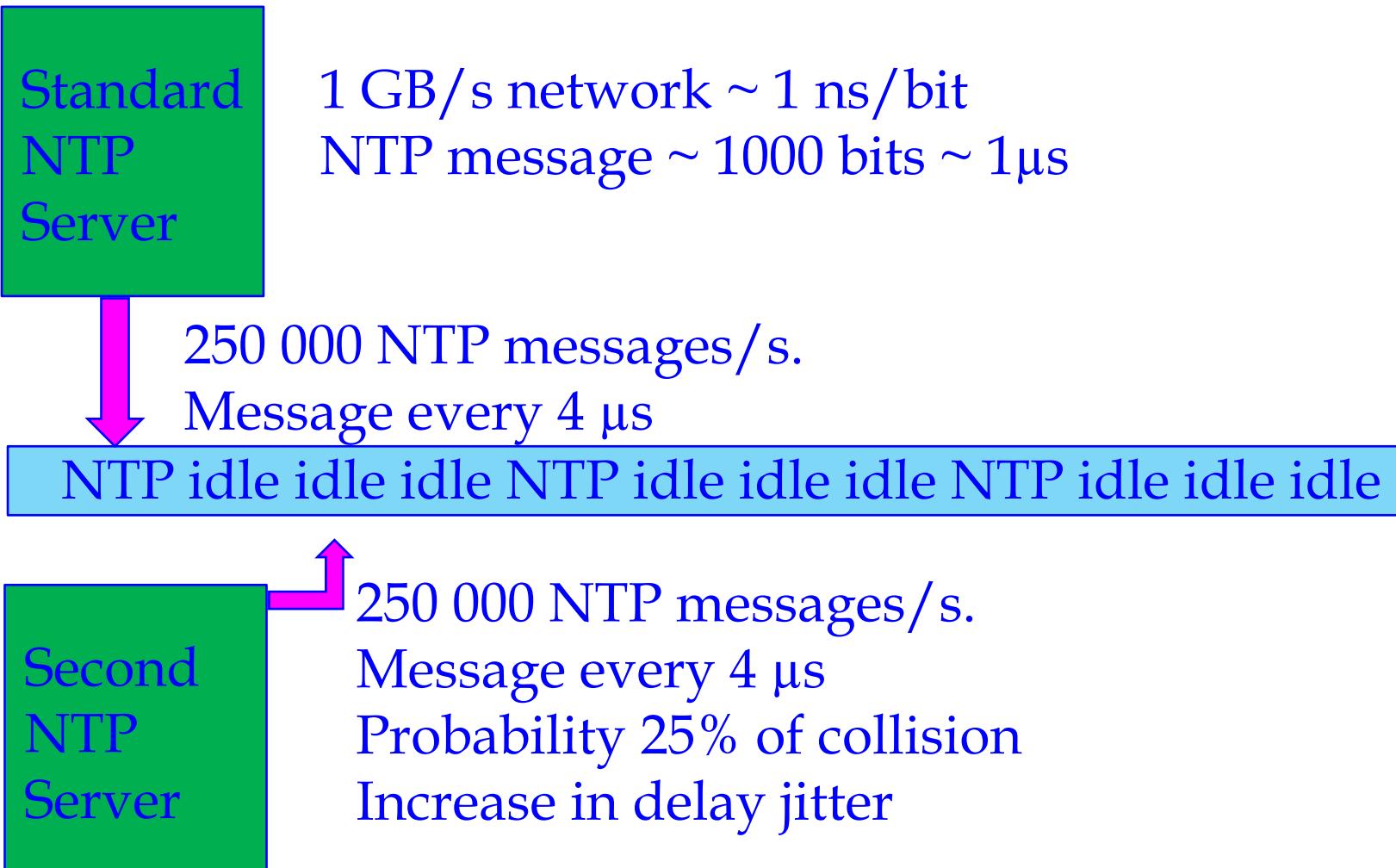


1 GB/s network  $\sim$  1 ns/bit

NTP message  $\sim 1000$  bits  $\sim 1\mu\text{s}$

Capacity  $\sim 10^6$  messages/second

# Multiple servers, 1 Gb/s network



## Multiple servers - 2

- Significant probability of a collision when multiple servers that run asynchronously share network bandwidth.
- Collisions increase jitter in network delay
  - Decrease accuracy of time service
- Problem does not happen when a single server is fast enough to respond to all of the requests

# FPGA Hardware and development system

- Numato Systems Mimas A7 board
  - Artix 50T FPGA
- Design uses
  - 1378 LUTs
  - 1478 Slice Registers
  - 1 Block RAM tile
- Software is Xilinx Vivado, ver 2020.1
- **Details are for identification only and no endorsement is implied.**

Thank you